NCV4274C

400 mA Low Dropout Voltage Regulator

Description

The NCV4274C is a precision micro−power voltage regulator with an output current capability of 400 mA available in the DPAK package.

The output voltage is accurate within ±2.0% with a maximum dropout voltage of 0.5 V with an input up to 40 V. Low quiescent current is a feature drawing only 130 μA with a 1 mA load. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

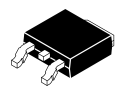
Features

- 3.3 V, 5.0 V, ±2.0% Output Options
- Low 130 μA Quiescent Current at 1 mA load current
- 400 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage with Respect to GND
  - −42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Very Low Dropout Voltage
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These are Pb−Free Devices

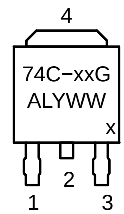
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAMS



DPAK
DT SUFFIX
CASE 369C



1	Input
2, 4	Ground
3	Output

xx	= 33 (3.3 V)
	= 50 (5.0 V)
A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

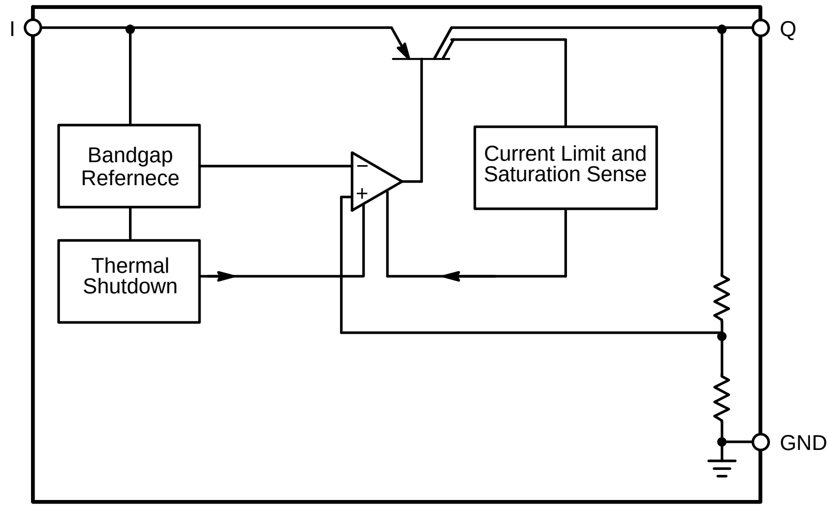


Figure 1. Block Diagram

Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	Input; Bypass directly at the IC a ceramic capacitor to GND.
2,4	GND	Ground
3	Q	Output; Bypass with a capacitor to GND.

ABSOLUTE MAXIMUM RATINGS

Pin Symbol, Parameter		Symbol	Condition	Min	Max	Unit
I, Input−to−Regulator	Voltage	V_I		−42	45	V
	Current	I_I		Internally Limited	Internally Limited	
I, Input peak Transient Voltage to Regulator with Respect to GND (Note 1)		V_I			60	V
Q, Regulated Output	Voltage	V_Q	$V_Q = V_I$	−1.0	40	V
	Current	I_Q		Internally Limited	Internally Limited	
GND, Ground Current		I_{GND}		−	100	mA
Junction Temperature Storage Temperature		T_J T_{Stg}		−40 −50	150 150	°C °C
ESD Capability, Human Body Model (Note 2)		ESD_{HB}		4		kV
ESD Capability, Machine Model (Note 2)		ESD_{MM}		200		V
ESD Capability, Charged Device Model (Note 2)		ESD_{CDM}		1		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class C.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD CDM tested per EIA/JES D22/C101, Field Induced Charge Model

OPERATING RANGE

Parameter	Symbol	Condition	Min	Max	Unit
Input Voltage (5.0 V Version)	V_I		5.5	40	V
Input Voltage (3.3 V Version)	V_I		4.5	40	V
Junction Temperature	T_J		−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL RESISTANCE

Parameter		Symbol	Condition	Min	Max	Unit
Junction−to−Ambient	DPAK	R_{thja}		−	112.3 (Note 3)	°C/W
Junction−to−Case	DPAK	R_{thjc}		−	5.8	°C/W

3. 1 oz copper, 100 mm^2 copper area, single−sided FR4 PCB.

Pb−FREE SOLDERING TEMPERATURE AND MSL

Parameter		Symbol	Condition	Min	Max	Unit
Pb−Free Soldering, (Note 4) Reflow (SMD styles only),	Pb−Free	T_{sld}	60s − 150s Above 217s 40s Max at Peak	−	265 pk	°C
Moisture Sensitivity Level		MSL	DPAK	1	−	

4. Per IPC/JEDEC J−STD−020C

ELECTRICAL CHARACTERISTICS
−40°C < T_J < 150°C; V_I = 13.5 V unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
REGULATOR						
Output Voltage (5.0 V Version)	V_Q	5 mA < I_Q < 400 mA 6 V < V_I < 28 V	4.9	5.0	5.1	V
Output Voltage (5.0 V Version)	V_Q	5 mA < I_Q < 200 mA 6 V < V_I < 40 V	4.9	5.0	5.1	V
Output Voltage (3.3 V Version)	V_Q	5 mA < I_Q < 400 mA 4.5 V < V_I < 28 V	3.23	3.3	3.37	V
Output Voltage (3.3 V Version)	V_Q	5 mA < I_Q < 200 mA 4.5 V < V_I < 40 V	3.23	3.3	3.37	V
Current Limit (All Versions)	I_Q	V_Q = 90% V_{QTYP}	400	600	–	mA
Quiescent Current	I_q	I_Q = 1 mA V_Q = 5.0 V V_Q = 3.3 V I_Q = 250 mA V_Q = 5.0 V V_Q = 3.3 V I_Q = 400 mA V_Q = 5.0 V V_Q = 3.3 V	 – – – – – –	 125 125 5 5 10 10	 250 250 15 15 35 35	 μA μA mA mA mA mA
Dropout Voltage 5.0 V Version	V_{DR}	I_Q = 250 mA, $V_{DR} = V_I − V_Q$ V_I = 5.0 V	 –	 250	 500	 mV
Load Regulation (3.3 V and 5 V Versions)	ΔV_Q	I_Q = 5 mA to 400 mA	–	3	20	mV
Line Regulation (3.3 V and 5 V Versions)	ΔV_Q	ΔV_I = 12 V to 32 V I_Q = 5 mA	–	4	25	mV
Power Supply Ripple Rejection	P_{SRR}	fr = 100 Hz, V_r = 0.5 V_{PP}	–	60	–	dB
Thermal Shutdown Temperature*	T_{SD}	I_Q = 5 mA	150	–	210	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Guaranteed by design, not tested in production

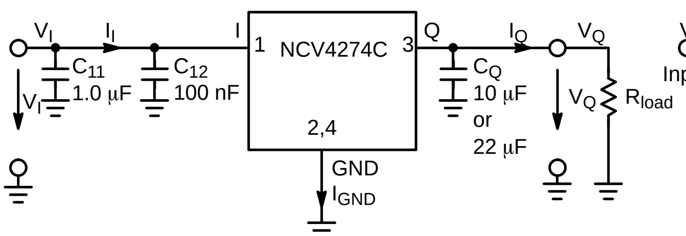


Figure 2. Measuring Circuit

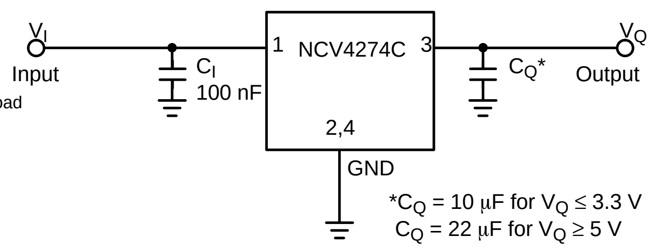


Figure 3. Application Circuit

TYPICAL CHARACTERISTIC CURVES − 5 V VERSION

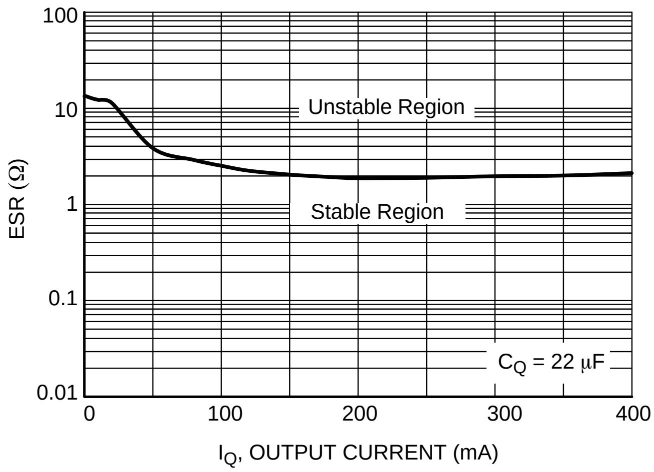


Figure 4. Output Stability with Output Capacitor ESR

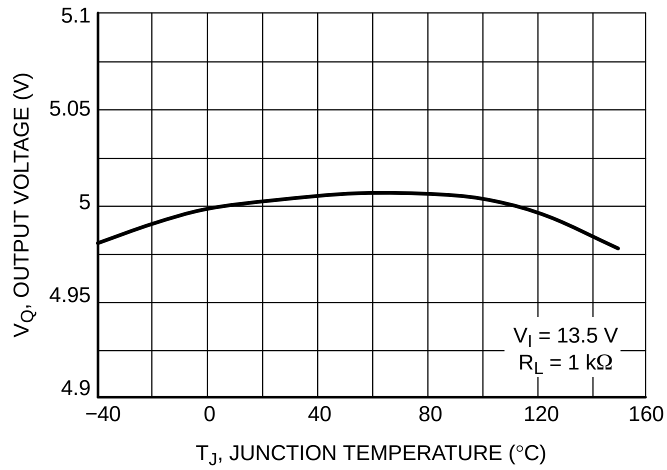


Figure 5. Output Voltage vs. Junction Temperature

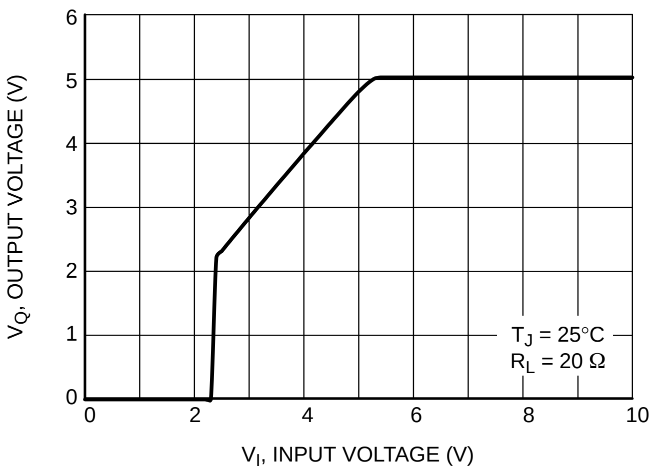


Figure 6. Output Voltage vs. Input Voltage

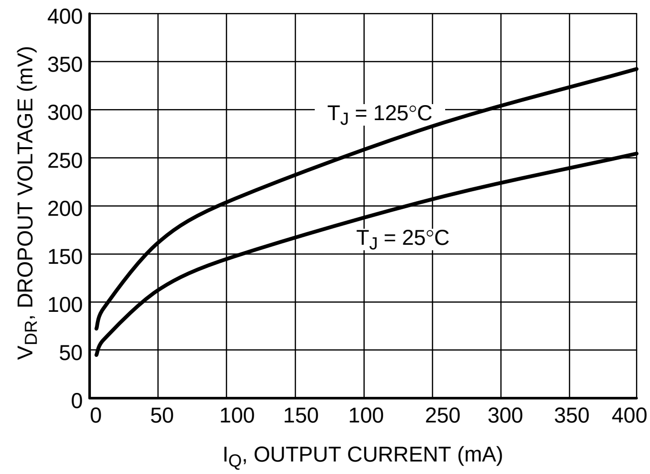


Figure 7. Dropout Voltage vs. Output Current

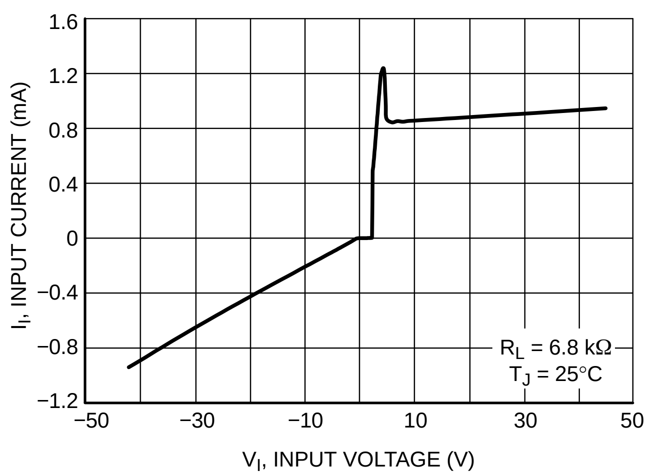


Figure 8. Input Current vs. Input Voltage

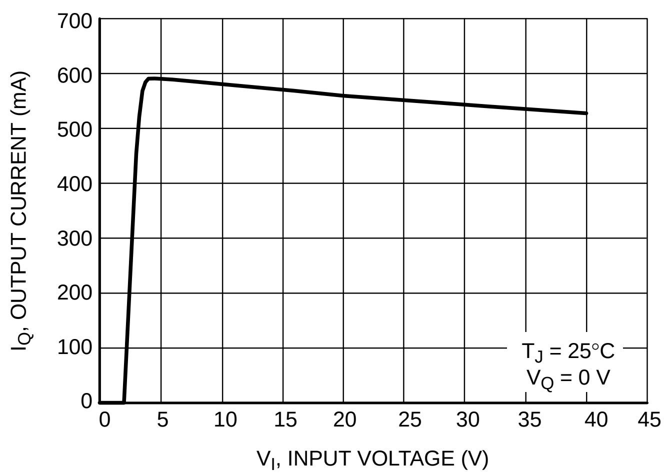


Figure 9. Maximum Output Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES − 5 V VERSION

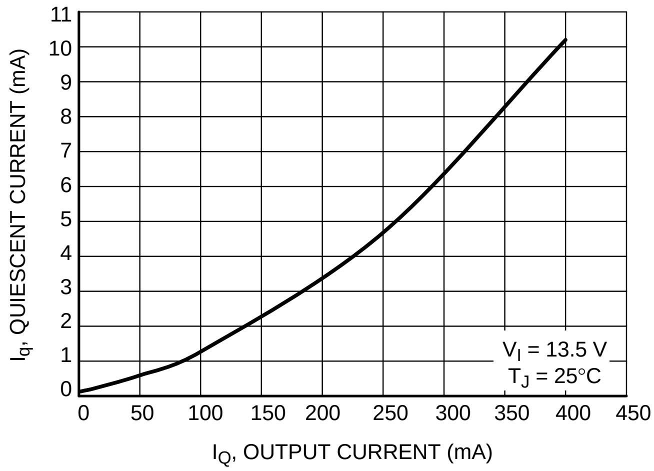


Figure 10. Quiescent Current vs. Output Current (High Load)

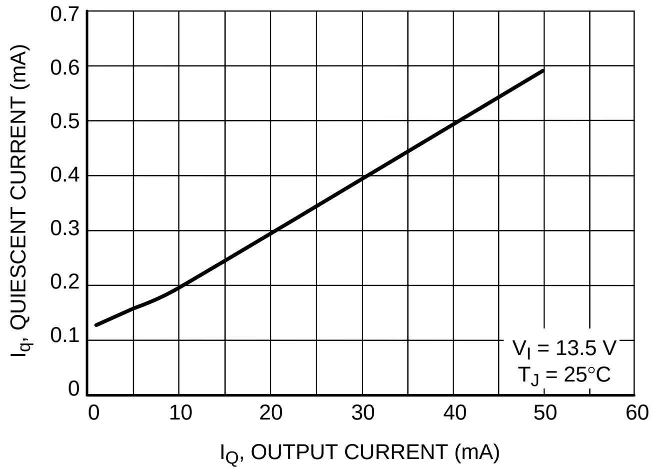


Figure 11. Quiescent Current vs. Output Current (Low Load)

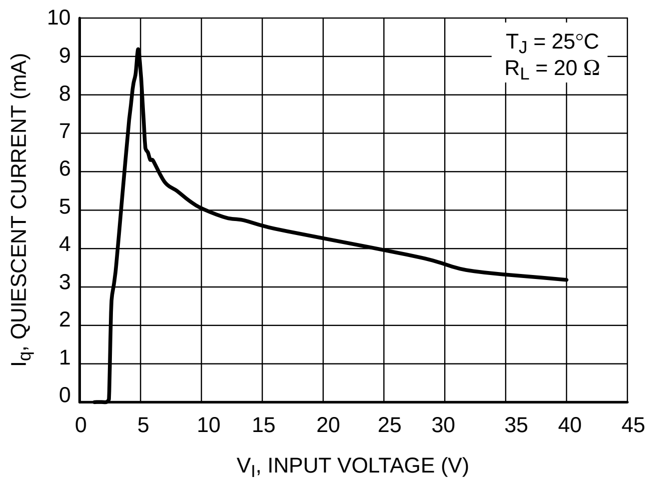


Figure 12. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES − 3.3 V VERSION

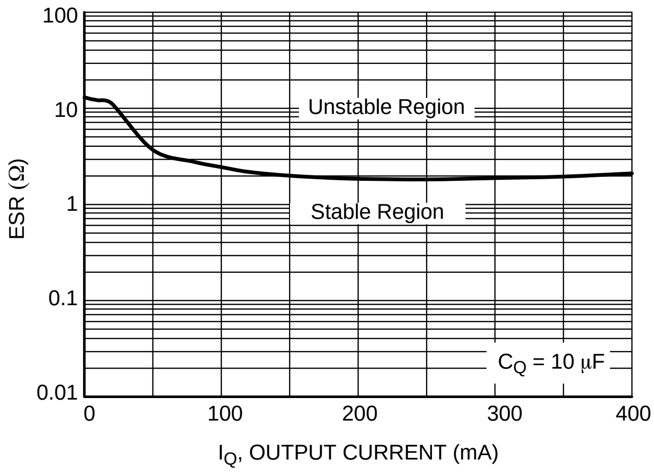


Figure 13. Output Stability with Output Capacitor ESR

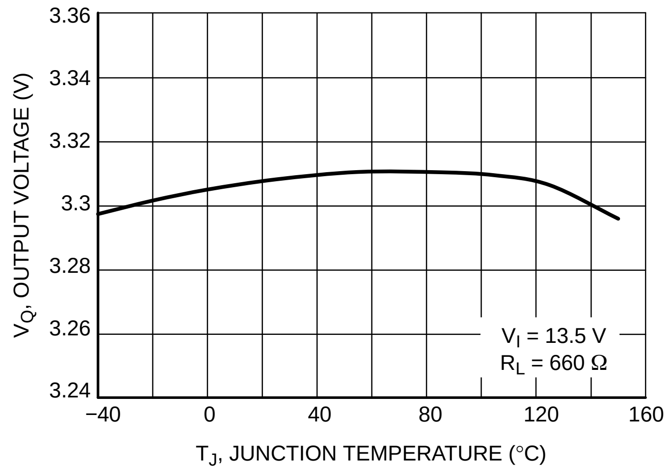


Figure 14. Output Voltage vs. Junction Temperature

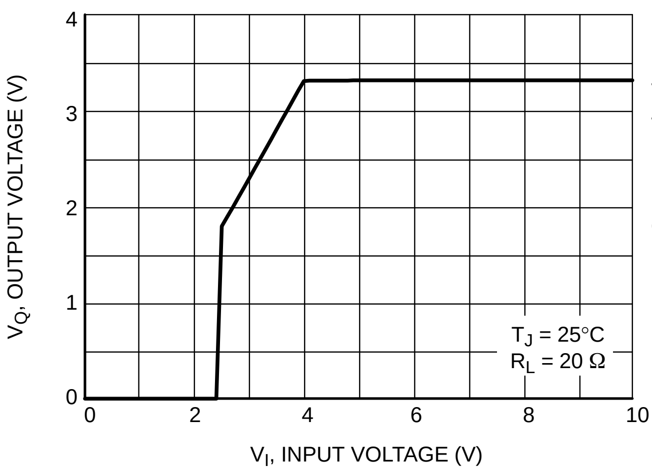


Figure 15. Output Voltage vs. Input Voltage

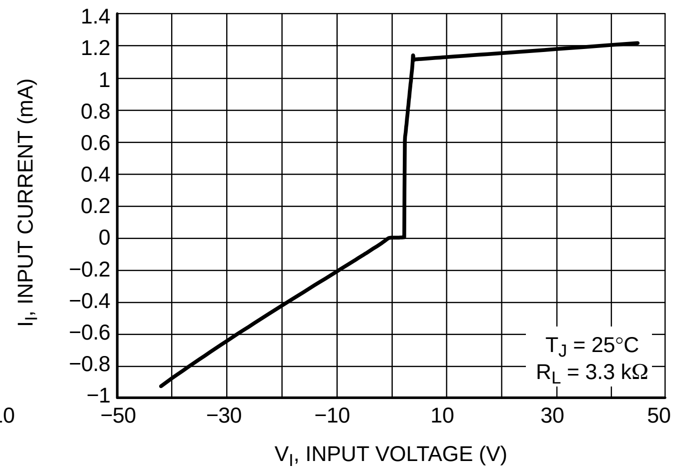


Figure 16. Input Current vs. Input Voltage

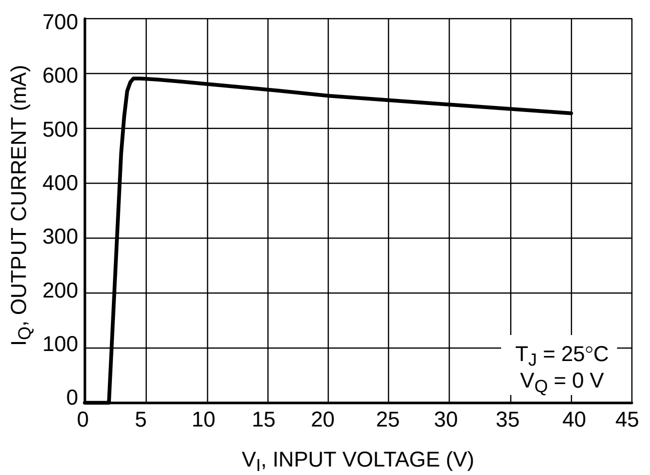


Figure 17. Maximum Output Current vs. Input Voltage

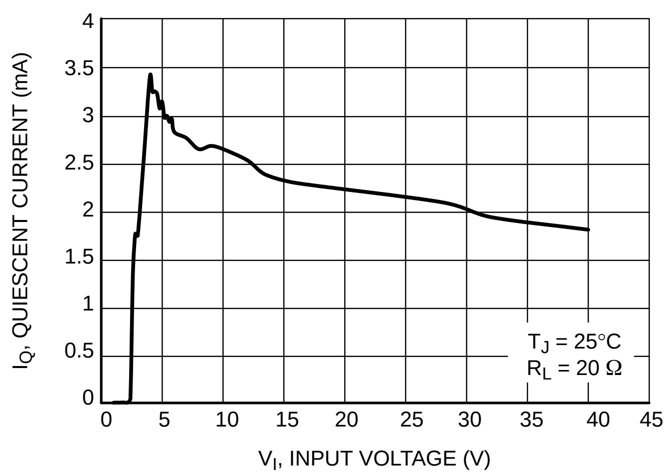


Figure 18. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES − 3.3 V VERSION

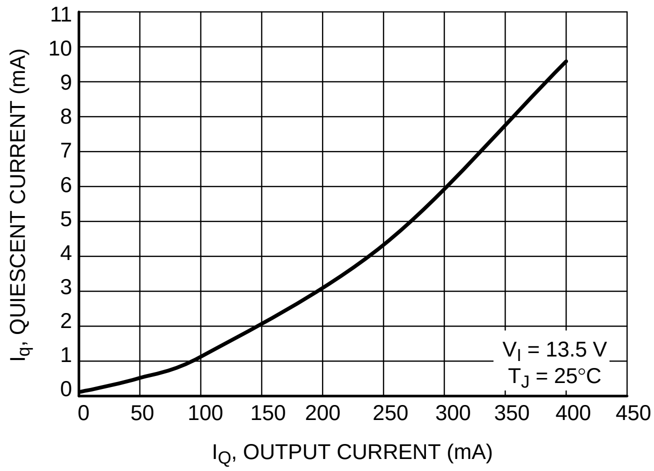


Figure 19. Quiescent Current vs. Output Current (High Load)

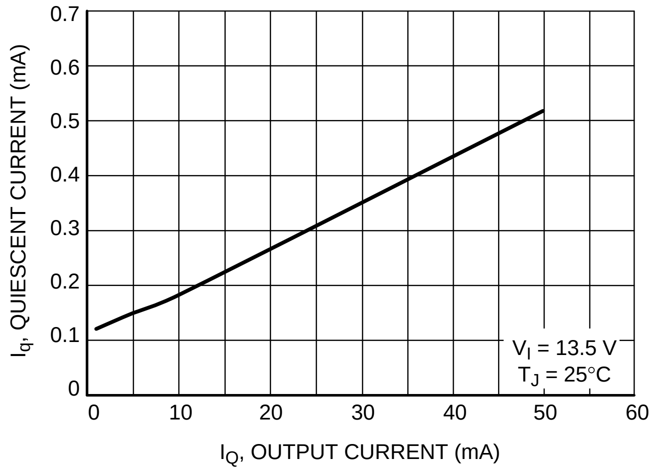


Figure 20. Quiescent Current vs. Output Current (Low Load)

APPLICATION DESCRIPTION

Output Regulator

The output is controlled by a precision trimmed reference and error amplifier. The PNP output has saturation control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

Stability Considerations

The input capacitor C_{I1} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{I2}.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_Q shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Actual Stability Regions are shown in a graphs in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad \text{(eq. 1)}$$

Where:

$V_{I(max)}$ is the maximum input voltage,
$V_{Q(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application, and
I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta_{JA}} = \frac{(150\,C - T_A)}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

Where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and
$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers.

Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

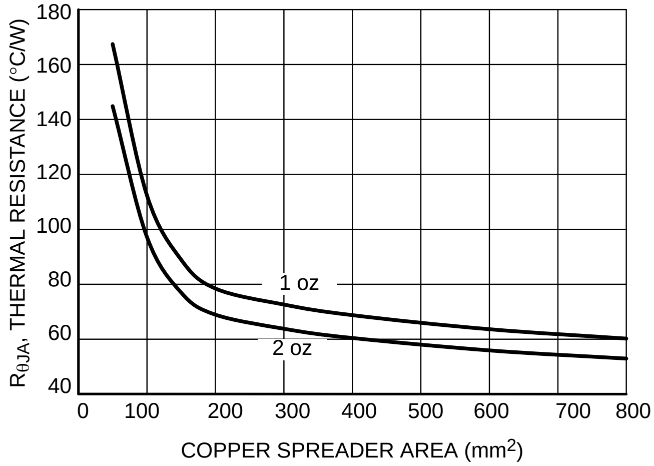


Figure 21. $R_{\theta JA}$ vs. Copper Spreader Area, DPAK 3−Lead

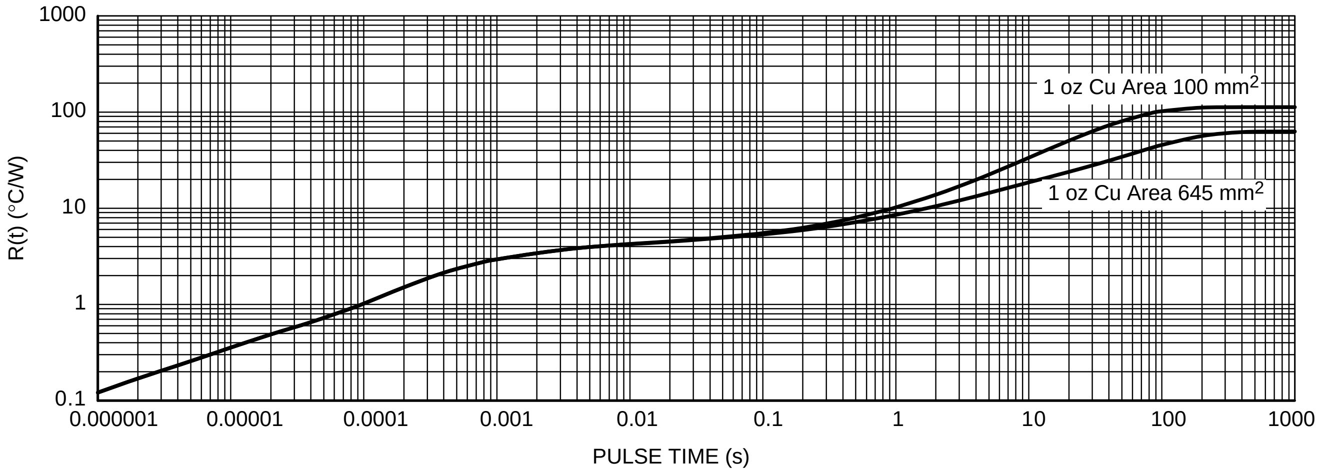


Figure 22. Single−Pulse Heating Curves, DPAK 3−Lead

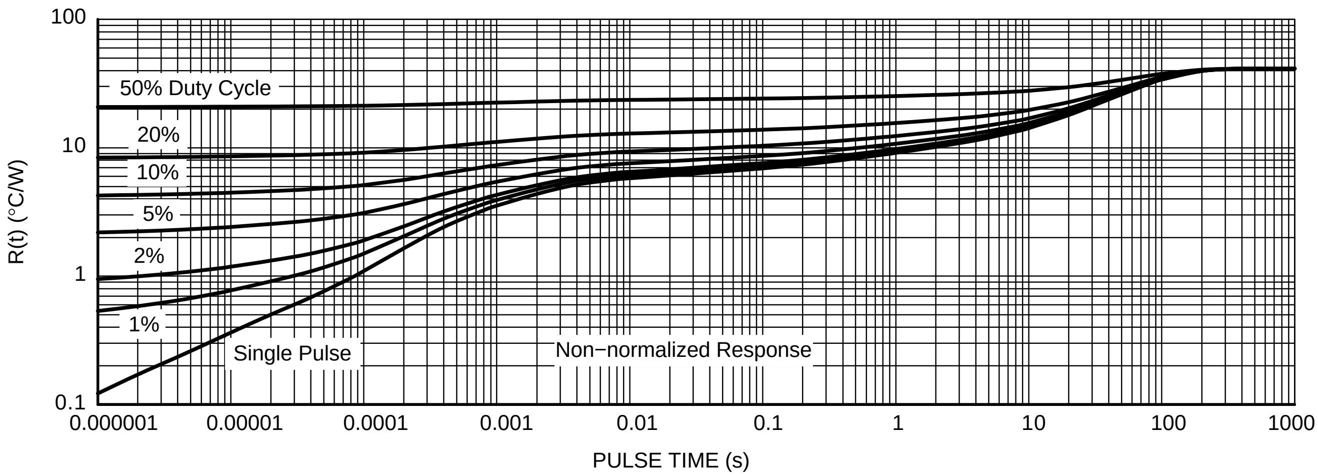


Figure 23. Duty Cycle for 1 $inch^2$ (645 mm^2) Spreader Board, DPAK 3−Lead

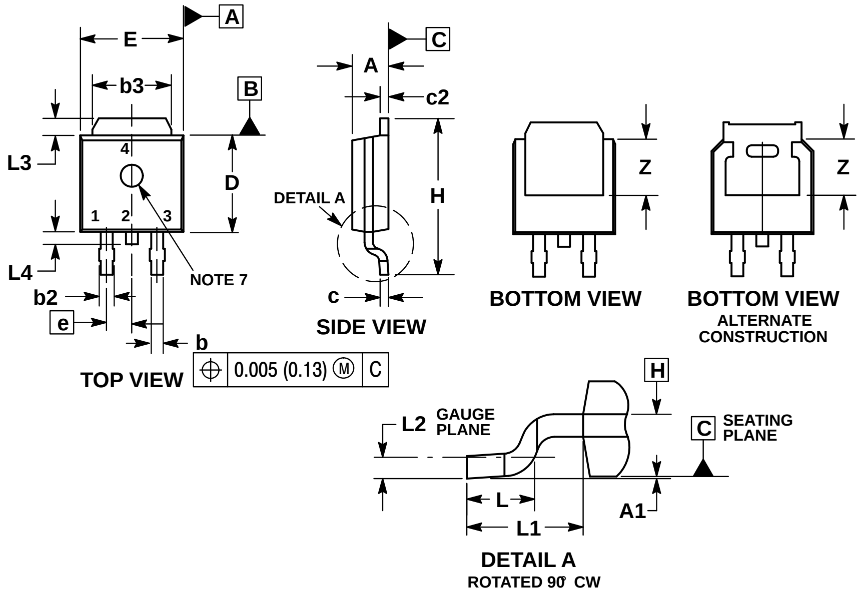
ORDERING INFORMATION

Device	Output Voltage Accuracy	Output Voltage	Package	Shipping†
NCV4274CDT50RKG	2%	5.0 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274CDT33RKG	2%	3.3 V	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

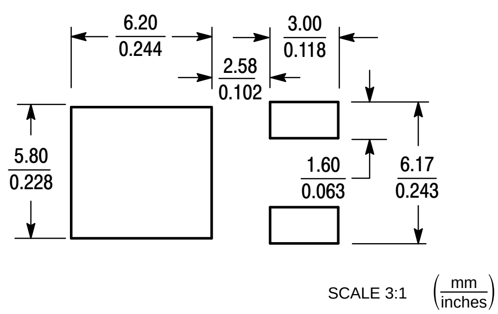
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	−−−	0.040	−−−	1.01
Z	0.155	−−−	3.93	−−−

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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